EE431 Quiz No

Date: Thursday, October 11, 2001
Time = 45 minutes
Text Books and Notes Only

(3) 1. Draw a block diagram (4 blocks in total all to be drawn as rectangles) for a circuit that implements a 6 input nand. Use only two types of blocks. The function of one block is that of a two input and gate. The function of the other is that of a three input nand gate. The block diagram will consist of four blocks along with interconnecting signals. Annotate the block diagram in complete detail so that it can be exactly translated into a structural description in Verilog HDL.

(3) 2. Provide an exact structural description (in the Verilog HDL) of the block diagram you gave in question 1.

(2) 3. Give examples of an implicit structural description and an explicit structural description using a two input and function.

(3) 4. Consider the circuit synthesized from the Verilog HDL given below.

```
module circuit_1 (a, b, c);
input [1:0] a,b;
output [3:0] c;

assign c = a + b;
```

If input a = 2'b11 and input b = 2'b10, what value would output c have?

(5) 5. Generate a Verilog HDL for a circuit that has a 3 bit input, x, and a one bit output, y, such that y = 1'b1 if and only if two of the three bits in x are ones.

(5) 6. Draw a schematic diagram of a circuit described by the Verilog HDL given below.

```
module circuit_2 (x,y);
input [3:0] x;
output [1:0] y;

reg [1:0]  y;

always @ (x)
   casex (x)
   4'b1xxx : y=2'b10;
   4'bx1xx : y=2'b01;
   4'bxx1x : y=2'b10;
   4'bxxx1 : y=2'b01;
   default : y=2'b00;
   endcase
endmodule
```

(4)

7. Draw a schematic diagram of a circuit described by the Verilog HDL given below. Use a d flip flop that has asynchronous set and clear inputs, both active high, with set overriding clear when both are active.

```
module circuit_3 (clk, x1, x2, x3, y);
input clk, x1, x2, x3;
output y;
reg y;

always @ (posedge clk or posedge x1)
if (x1==1'b1) y = 1'b0;
else if (x2 == 1'b1) y = 1'b1;
else y = x3;

endmodule
```

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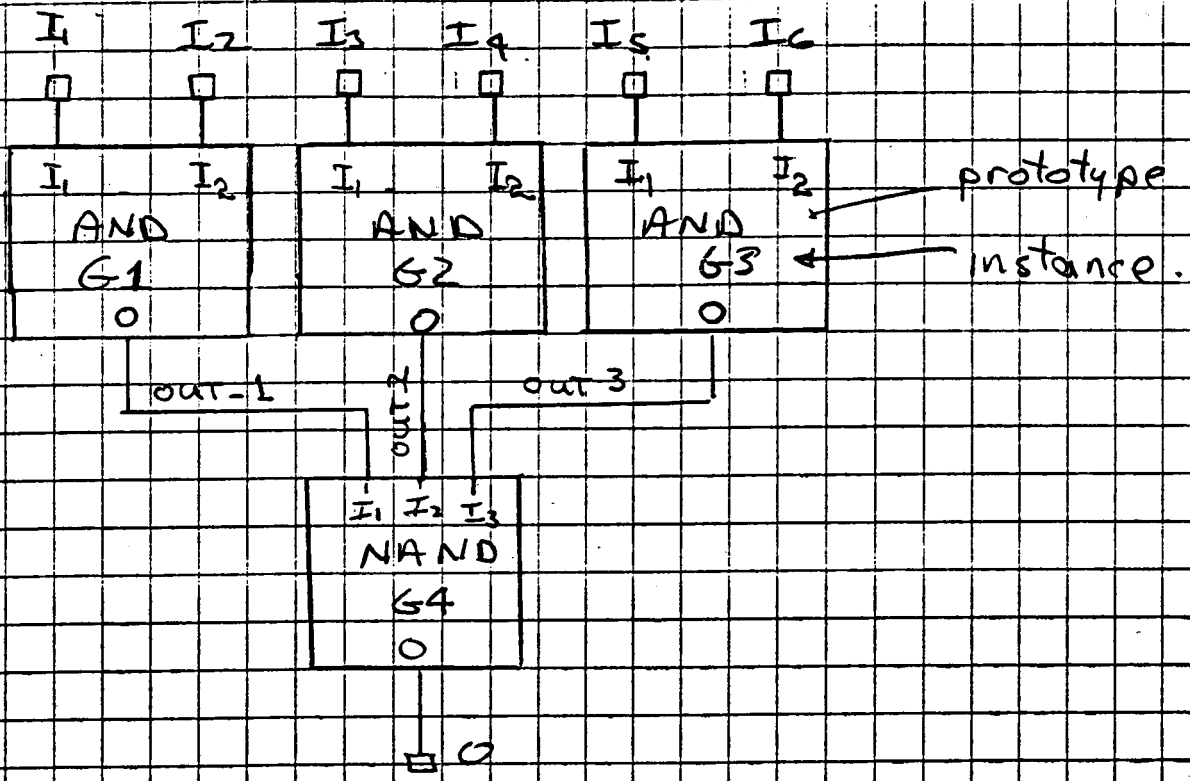
SOLUTION

1.




```
module nand_12 (I1, I2, I3, I4, I5, I6,
                O);
input I1, I2, I3, I4, I5, I6;
output O;

wire out_1, out_2, out_3;

AND G1 (.I1(I1), .I2(I2), .O(out_1));
AND G2 (.I1(I3), .I2(I4), .O(out_2));
AND G3 (.I1(I5), .I2(I6), .O(out_3));

NAND G4 (.I1(out_1), .I2(out_2), .I3(out_3), .O(O));

endmodule.
```

2. Implicit structural description of a two input and

```
assign c = a & b;
```

Explicit description

```
and G1 (c, a, b)
```

← instantiation

3.

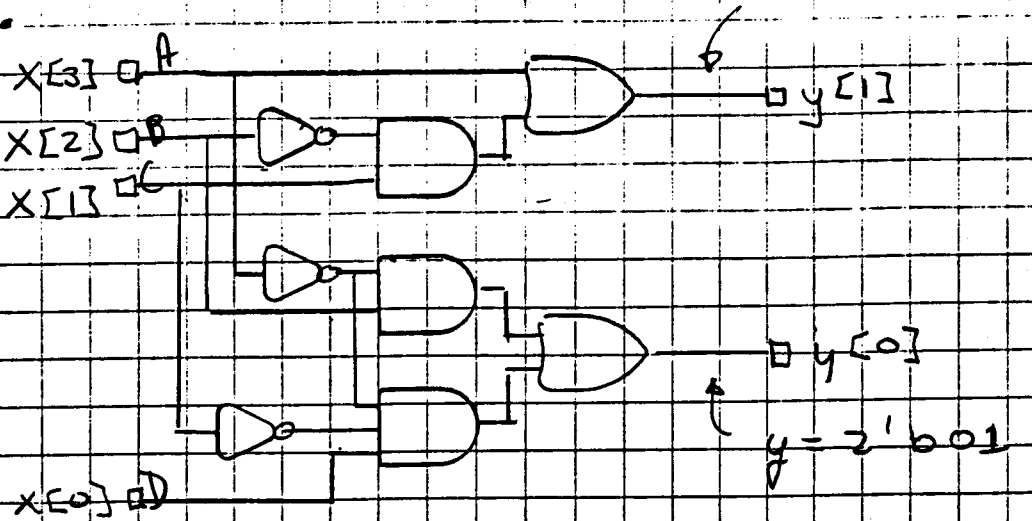
$$\begin{array}{r} a \\ +\,b \\ \hline \end{array} = \begin{array}{r} 11 \\ +\,10 \\ \hline 101 \end{array}$$

∴ c = 4'b0101

4.

```
module two-bit-detector (x, y);
input [2:0] x;
ouput y;
reg y;
always @ (x)
  if((x == 3'b110) || (x==3'b101) || (x==3'b011))
    y = 1'b1;
  else y = 1'b0;
endmodule
```

5.



6.